REMARKS

Claims 1 and 2 are pending in the present application. Claims 1 and 2 are herein amended. New claims 3 and 4 have been added. No new matter has been entered. In light of the forgoing amendments, and the following remarks, Applicants earnestly solicit favorable reconsideration.

Claim Rejections Under 35 U.S.C. § 112 second paragraph:

Claims 1 and 2 were rejected under 35 U.S.C. § 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant has amended independent claims 1 and 2 and respectfully submit that the presented claims comply with 35 U.S.C. § 112 second paragraph.

On the Merits

Claim Rejections Under 35 U.S.C. § 102(e):

Claims 1 and 2 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Baker* (US Patent 6,661,181).

Differences between Baker and the Invention of Claims 1 and 2

In the receiver as recited in claim 1, the count value of the number-of-packet-arrivals counting means is updated (plus "1") each time the packet transmitted for each predetermined time interval from the transmitter is received, the count value of the number-of-packet-arrivals

counting means is multiplied by a packet transmission time interval determined on the side of the transmitter, and a predetermined offset value is added to the result of multiplication, thereby generating a virtual time on the side of the transmitter. Furthermore, the time on the side of the receiver is synchronized with the time on the side of the transmitter by a PLL circuit on the basis of the virtual time on the side of the transmitter. Then, when the time on the side of the receiver coincides with the time on the side of the transmitter which is added to the received packet, the packet is decoded.

The receiver 8 as described in *Baker* (see Figs. 4 and 8), upon receipt of the first data packet of a data stream, stores the time of the receipt on the receiver side (internal time), t_1, and the timestamp in the first data packet, T_1. The time on the side of the receiver is obtained by the cycle time register 83 (see Fig. 8). This cycle time register 83 and the cycle time register 65 (see Fig. 6) of the transmitting device 6 (see Figs. 4 and 6) are synchronized in frequency. The receiver 8 of *Baker* is **not** provided with a PLL circuit for synchronizing the time on the transmitter side with the time on the receiver side.

An offset value Δ is added to the time t_1. Where T_0 is an adding result, $T_0 = t_1 + \Delta$. T_0 is held by the latch 92. When the time on the receiver side reaches T_0 ($= t_1 + \Delta$), the first data packet is output from the buffer 86 and sent to the MPEG decoder 96. That is, the first data packet is decoded when the time Δ elapses after it is received.

Upon receipt of each succeeding data packet of the data stream, the timestamp T_n in the packet is stored. Then, $(T_n - T_1)$ is calculated. The n-th packet in the data stream is output from the buffer 86 when the time on the receiver side obtained by the cycle time register 83 (see Fig. 8) reaches $\{T_0 + (T_n - T_1)\}$ (which is determined by the comparator 93), and then sent to the MPEG decoder 96.

T_0 $(= t_1 + \Delta)$ is calculated by the adder circuit 90 shown in Fig. 8. $(T_n - T_1)$ is calculated by the subtractor circuit 89 of Fig. 8. $\{T_0 + (T_n - T_1)\}$ is calculated by the adder circuit 95 of Fig. 8.

The receiver 8 of *Baker* does not update the count value of the number-of-packet-arrivals counting means (plus "1") each time the packet transmitted for each predetermined time interval from the transmitter is received, as in the receiver of claim 1. The receiver 8 of *Baker* also fails to multiply the count value of the number-of-packet-arrivals counting means by a packet transmission time interval determined on the side of the transmitter, as in the receiver of claim 1.

Furthermore, the receiver 8 of *Baker* does not comprise the PLL circuit for synchronizing the time on the side of the receiver 8 with the time on the side of the transmitter.

In brief, *Baker* fails to disclose the following features (a1) to (a4) as recited in claim 1:

(a1) number-of-packet-arrivals counting means for updating a count value each time the packet transmitted for each predetermined time interval from the transmitter is received,

(a2) multiplying means for multiplying the count value of the number-of-packet-arrivals counting means by a packet transmission time interval determined on the side of the transmitter,

(a3) adding means for generating a virtual time on the side of the transmitter by adding a predetermined offset value to a result of multiplication by the multiplying means,

(a4) means for synchronizing the time on the side of the receiver with the time on the side of the transmitter by a PLL circuit on the basis of the virtual time on the side of the transmitter obtained by the adding means.

The receiver 8 of *Baker* does not update the count value of the number-of-packet-arrivals counter (plus "1") each time the packet transmitted for each predetermined time interval from the transmitter is received, as in the receiver of claim 2. The receiver 8 of *Baker* also fails to multiply the count value of the number-of-packet-arrivals counter by a packet transmission time interval determined on the side of the transmitter, as in the receiver of claim 2.

Furthermore, the receiver 8 of *Baker* does not comprise the PLL circuit for synchronizing the time on the side of the receiver 8 with the time on the side of the transmitter.

In brief, *Baker* fails to disclose the following features (b1) to (b4) as recited in claim 2:

(b1) a number-of-packet-arrivals counter for updating a count value each time the packet transmitted for each predetermined time interval from the transmitter is received,

(b2) a multiplier for multiplying the count value of the number-of-packet-arrivals counter by a packet transmission time interval determined on the side of the transmitter,

(b3) an adder for generating a virtual time on the side of the transmitter by adding a predetermined offset value to a result of multiplication by the multiplier,

(b4) a circuit for synchronizing the time on the side of the receiver with the time on the side of the transmitter by a PLL circuit on the basis of the virtual time on the side of the transmitter obtained by the adder.

Differences between Baker and the Invention of Claims 3 and 4

The transmitting device 6 of *Baker* (see Figs. 4 and 6) comprises the oscillator 66, the Cycle Start Processor 67, the Cycle time Register 65, the CIP processor 61, the timestamp module 62, the IEEE 1394 processor 63 and the buffer 64.

The timestamp module 62 adds the transmission timestamp to a packet obtained by the CIP processor 61. The packet with the timestamp added thereto is supplied via the IEEE 1394 processor 63 and the buffer 64 to the output terminal 69 connected to the bus 1.

The Cycle Time Register 65 produces a clock which is capable of adding a timestamp to data packets, and then provides the clock to the timestamp module 62.

The transmitter as recited in claims 3 and 4 includes the following feature (c1) to (c4):

(c1) the time information adding circuit adding to the packet outputted from the coding device transmitter-side time information representing the time on the side of the transmitter when the packet is outputted from the coding device,

(c2) the transmission buffer holding the packet to which the transmitter-side time information is added by the time information adding circuit, outputting the packet upon receipt of a transmission instruction, and erasing the racket which has been transmitted upon receipt of a packet erasure instruction,

(c3) the clock generation circuit generating a clock, and

(c4) the transmission time counter generating the transmitter-side time information based on the clock generated from the clock generation circuit to provide the transmitter-side time information for the time information adding circuit, and outputting the transmission instruction to the transmission buffer at predetermined time intervals.

Baker fails to describe in detail the timing at which the packet held in the buffer 64 is output. Baker is also completely silent about erasing the packet held in the buffer 64.

Therefore, *Baker* fails to disclose the features (c2) and (c4) among the aforementioned features (c1) to (c4) of claims 3 and 4.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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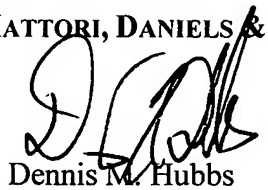

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